Claim Amendments

1. (Previously Presented) A memory device comprising:

a storage array comprised of a plurality of memory cells;

an interface buffer coupled to the storage array, and having a first interface to couple the memory device to a first memory bus to couple the memory device to a memory controller;

memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array under at least one of conditions comprising in response to a command from the memory controller and during an idle period associated with transactions carried out by the memory controller on the first memory bus that involve the storage array; and

bus error logic associated with the interface buffer to carry out a check for bus errors in transactions across the first memory bus between the memory controller and the first interface.

2. (Previously Presented) The memory device of claim 1, wherein the memory error logic is a component of the interface buffer, and wherein the memory device is comprised of a circuitboard to which is attached at least one integrated circuit that comprises the storage array and at least one integrated circuit that comprises the interface buffer.

3. (Previously Presented) The memory system device of claim 1, wherein, the first memory bus provides a point-to-point connection between the memory device and the memory controller, the interface buffer has a second interface to couple the memory device to a second memory bus to provide a point-to-point connection between the memory device and another memory device, and the interface buffer passes through bus activity between the first and second memory busses that does not involve the storage array.

4. (Previously Presented) The memory device of claim 3, wherein both a transfer of data between the memory controller and the first interface of the interface buffer and a transfer of data between the second interface of the interface buffer and the another memory device occur with data transmitted in a packets.

5-9. (Canceled)

10. (Previously Presented) The memory device of claim 3, wherein the memory error logic corrects a memory error, if a memory error is detected and is correctable; and the memory error logic transmits a signal to the memory controller if a memory error is detected and is not correctable.

11. (Canceled).

12. (Currently Amended) The memory device of claim ~~11~~ 1, wherein a transaction across the first memory bus entails the transmission of data in a packet with CRC information, and the bus error logic examines the data and the CRC information to check for an occurrence of a bus error.

13-26. (Canceled).

27. (Previously Presented) A computer system comprising:

a processor;

a disk storage device coupled to the processor

a memory controller coupled to the processor;

a first memory bus coupled to the memory controller;

a first memory device having a first storage array comprised of a plurality of memory cells and a first interface buffer coupled within the first memory device to the first storage array, wherein the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface, a first memory error logic to carry out a check for memory errors within the first storage array under at least one of conditions comprising in response to a first command from the memory controller and during an idle period associated with transactions carried out by the memory controller on the first memory bus that involve the first storage array, and a first bus error logic associated with the first interface buffer to carry out a check for bus errors in transactions on the first memory bus between the memory controller and the first interface.

28-38. (Canceled)

39. (Previously Presented) The memory device of claim 1, wherein during the idle period, there are no transactions carried out by the memory controller on the first memory bus that involve the storage array.

40. (Previously Presented) The computer system of claim 27, wherein during the idle period, there are no transactions carried out by the memory controller on the first memory bus that involve the first storage array.

41. (Canceled).

42. (Previously Presented) The computer system of claim 27, wherein the first interface buffer further comprises a second interface.

43. (Previously Presented) The computer system of claim 42, further comprising:

a second memory bus coupled to the second interface; and

a second memory device having a second storage array comprised of a plurality of memory cells and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second memory bus forming a point-to-point connection between the third interface and the second interface, a second memory error logic to carry out a check for memory errors within the second storage array under at least one of conditions comprising in response to a second command from the memory controller and during an idle period associated with transactions carried out by the memory controller on the second memory bus that involve the second storage array, and a second bus error logic associated with the second interface buffer to carry out a check for bus errors in transactions across the second memory bus between the memory controller and the second interface.

44. (Previously Presented) The computer system of claim 43, wherein during the idle period, there are no transactions carried out by the memory controller on the second memory bus that involve the second storage array.

45-48. (Canceled).